CSE 2600 - Homework 2A

Always show all work for full credit.

1. Review: Fill in the missing values in the following table (all values are unsigned)

Binary	Decimal	Hex
1010110		
		0x1AB
	225	

2. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

3. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

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4. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

5. Write a Boolean equation in sum-of-products canonical form for:

A	B	C	D	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

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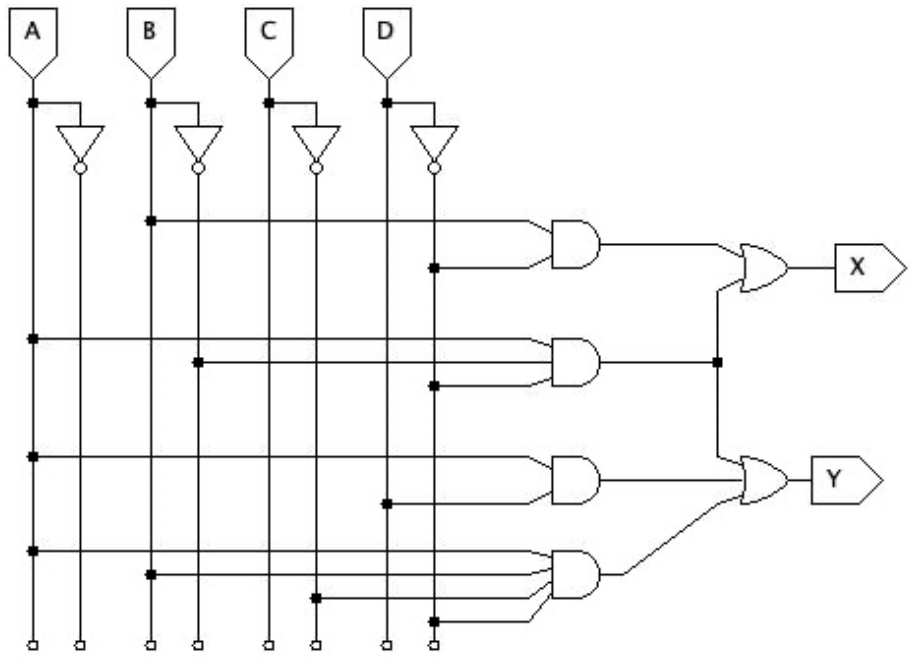
6. Implement the below with only NAND gates (it's the same function in 4).
   Although it may not be the minimum number of gates possible, you can identify how NANDs can be used to represent ANDs, Ors, and NOTs, and then use simple substitution in a Sum-of-Products equation.
   Sketch the circuit or use JLS to create the circuit diagram:

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

7. Write the Boolean equations for the circuit below (no need to minimize: give the exact equations implemented in the circuit):



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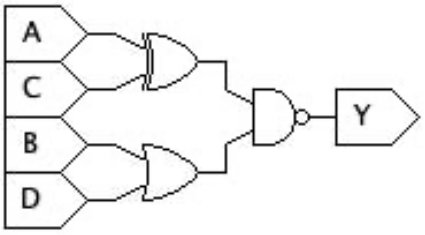
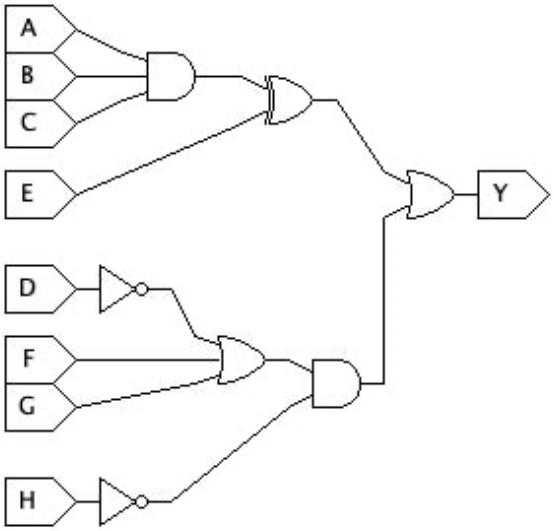
For the next four problems assume the propagation delays are:

Gate	t_{pd} (ps)
NOT	6
2-input NAND	22
3-input NAND	27
4-input NAND	37
2-input NOR	25
3-input NOR	35
2-input AND	25
3-input AND	36
4-input AND	42
2-input OR	25
3-input OR	44
4-input OR	48
2-input XOR	20

8. Determine the propagation delay of:



9. Determine the propagation delay of:



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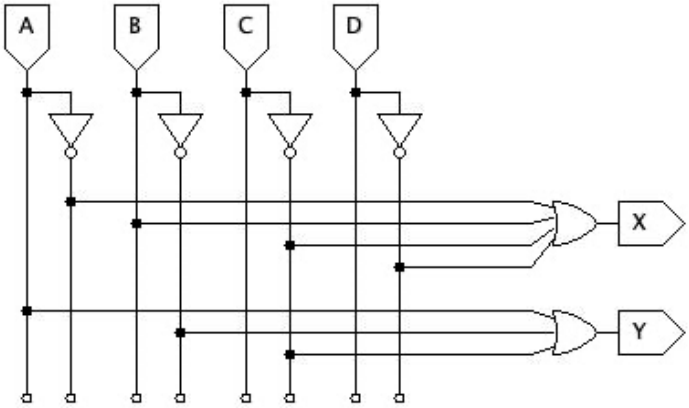
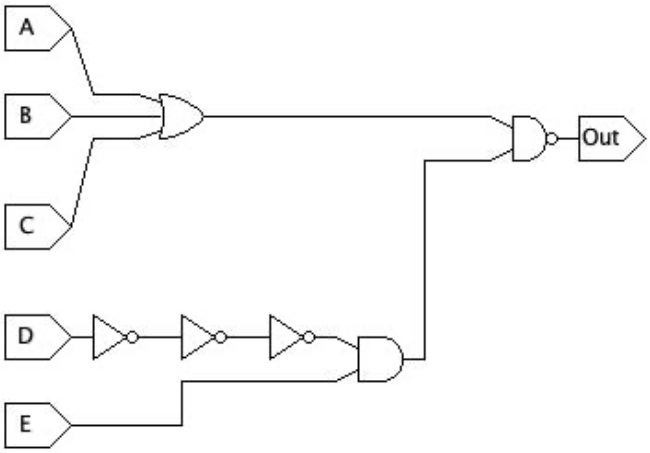
10. Determine the propagation delay of:



11. Determine the propagation delay of:



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12.1 Consider adding 2-digit binary numbers, A and B, to produce the 2-bit result, S, and a carry-out, C:

$$\begin{array}{cccc} & A_1 & A_0 \\ + & B_1 & B_0 \\ C & S_1 & S_0 \end{array}$$

Develop the truth table and sum-of-products equations for adding the two, 2-bit numbers and produce the 3-bits of the result.

12.2 ***Download the JLS starter file from the assignment page*** and complete the circuit. Note that it uses 2-bit inputs for A and B. You test all possible combinations of inputs to confirm your 2-bit adder works correctly. Hints:

- Think carefully about the structure of the truth table and the terms being used for each output.
- Some product terms can be reused for different outputs.
- JLS has parts called "named wires". Named wires can be used to organize your work and re-use common terms. Named wires have two parts: the source ("name a wire" is shown when you hover over the named wire part on the menu) and connections ("connect to a named wire"). You can use more than one of the "connect to a named wire" part to have a single wire connect multiple places without having a literal wire (line) running across the diagram. If you use named wires, try to name them with a name that describes their purpose.
- Some wires and parts have already been provided. They are intended to provide one tidy approach to laying out the circuit.
- This circuit uses multi-bit inputs and separates them into their individual bits (A0, A1, etc.) for you. Test signal values can be specified in decimal rather than binary. For example, A can be 0, 1, 2, or 3. When A is 2 its individual bits, A1 and A0, are 1 and 0 respectively. The bits of S are combined into a single, 2-bit output, which doesn't include C.
- Carefully think about test cases. A signal generator has already been provided.
- ***DO NOT change the names of either input or output ports.*** The Autograder depends on them being named as-is.
- ***DO NOT remove any of the parts already included in the file. You can add more (but should not add unnecessary parts)***

13. JLS problem: **See assignment page and use the provided starter file!**

$$O = \overline{A} \cdot \overline{B} \cdot C + B \cdot D$$

- ***DO NOT change the names of either input or output ports.*** The Autograder depends on them being named as-is.
- ***DO NOT remove any of the parts already included in the file. You can add more (but should not add unnecessary parts)***